

HIGH-SPEED SERIAL DATA TRANSCEIVER AND RELATED METHODS

ABSTRACT OF THE DISCLOSURE

A high-speed serial data transceiver includes multiple receivers and transmitters for receiving and transmitting multiple analog, serial data signals at multi-gigabit-per-second data rates. Each receiver includes a timing recovery system for tracking a phase and a frequency of the serial data signal associated with the receiver. The timing recovery system includes a phase interpolator responsive to phase control signals and a set of reference signals having different predetermined phases. The phase interpolator derives a sampling signal, having an interpolated phase, to sample the serial data signal. The timing recovery system in each receiver independently phase-aligns and frequency synchronizes the sampling signal to the serial data signal associated with the receiver. A receiver can include multiple paths for sampling a received, serial data signal in accordance with multiple time-staggered sampling signals, each having an interpolated phase.